Government of Karnataka

Department of Technical Education
Board of Technical Examinations, Bengaluru

Course Title: **Digital Electronics Lab-2**		Course Code	: **15EC36P**
Credits	: **3 Credits**	Semester	: **Third**
Teaching Scheme in Hrs (L:T:P)	: **0:2:4**	Course Group	: **Core**
Type of course	: **Tutorial + Practical**	Total Contact Hours	: **78**
CIE	: **25 Marks**	SEE	: **50 Marks**

Prerequisites

Knowledge of basics of digital electronics and number systems.

Course Objectives

To understand the working of various digital electronics circuits and to design and analyze simple logic circuits.

Course Outcomes

Course Outcome		CL	Linked Experiments	Linked PO	Teaching Hrs
CO1	Identify the various digital ICs and their specifications and applications.	***R/U/A***	Unit-1: Part A: E1	1,2,3,4,10	6
CO2	Apply the basic knowledge of digital electronics to design simple combinational circuits.	***R/U/A***	Unit-1: Part A: E2-9	1,2,3,4,10	24
CO3	Analyze the functions of flip-flops various flip-flops	***U/A***	Unit-1:Part B: E1-3	1,2,3,4,10	09
CO4	Construct and test simple sequential circuits and data converters	***R/U/A***	Unit-1: Part B: E4-12	1,2,3,4,10	27
CO5	Employ modern tools for the analysis, design and simulation of simple digital circuits.	***U/A***	Unit-2	1,2,3,4,10	03 and off-classes
CO6	Apply digital electronics concepts and comprehend the recent developments related to digital electronics.-mini project	***U/A***	Unit 2	1,2,3,4,5,8, 9,10	03 and off-classes
				Two CIE/IA Tests	**06**
				Total	**78**

Legend: E- Experiment, R-Remember, U-Understand, A-Application, CL-Cognitive Level, and PO-Program Outcome

Course-PO Attainment Matrix

Course	Programme Outcomes									
	1	2	3	4	5	6	7	8	9	10
Digital Electronics Lab-2	3	3	3	3	1	--	--	1	1	3

Level 3- Highly Addressed, Level 2-Moderately Addressed, Level 1-Low Addressed.

Method is to relate the level of PO with the number of hours devoted to the COs which address the given PO.

If ≥40% of classroom sessions addressing a particular PO, it is considered that PO is addressed at Level 3

If 25 to 40% of classroom sessions addressing a particular PO, it is considered that PO is addressed at Level 2

If 5 to 25% of classroom sessions addressing a particular PO, it is considered that PO is addressed at Level 1

If < 5% of classroom sessions addressing a particular PO, it is considered that PO is considered not-addressed.

Course Contents

Unit – 1: Tutorial and Practice 60 Hours

Sl. No.	Topic/Exercises	Duration (Hr.)
	Group A: Combinational Circuits	**24**
1	(i) Identify various IC (digital, analog, mixed) packages and families and learn to identify pin numbers in different packages. (ii) Practice handling of ICs with precautions and know IC soldering methods.	6
2	Verify the functionality of 2:1 or 4:1 multiplexer using suitable gates	3
3	Construct 4:1 multiplexer using 2:1 multiplexer IC and verify the operation.	3
4	Realise basic gates or simple logic expressions using multiplexer IC.	3
5	Verify the operation of 1:2 or 1:4 demultiplexer using suitable IC.	3
6	Verify the operation of BCD to Decimal decoder using suitable IC.	3
7	Construct and verify the circuit to translate BCD to decimal digits in seven-segment display using suitable IC	3
8	Verify the operation of decimal to BCD encoder using suitable IC.	3
9	Illustrate the storing and retrieving of data in RAM using suitable IC.	3
	Group B: Sequential Circuits	
1	Construct clocked SR FF using gates and verify its functionality.	3
2	Verify the TT of JK FF using IC 7476. Observe the role of preset and clear inputs.	3
3	Realize D-FF and T-FF using JK FF and observe the timing diagrams.	3
4	Move 3-bit or 4-bit data in SISO and PISO modes using FFs and tabulate the data movement in each mode.	3

5	Move or 4-bit data in SISO, SIPO, PIPO, PISO modes using suitable IC and tabulate the data movement in each mode.	3
6	Construct 3-bit ripple counter (both up and down separately) using flip-flop IC 7476 and verify its truth table	3
7	Configure IC 7490 as mod 10 counter and verify its truth table	3
8	Verify the operation of a 3-bit or 4-bit ring and Johnson's counter using suitable flip-flop IC	3
9	Construct astable multivibrator using timer IC 555 to generate square output waveform for a given frequency.	3
10	Construct monostable multivibrator using timer IC-555 to generate pulses of different ON periods.	3
11	Convert digital data to analog signal using suitable DAC IC and observe the output for various inputs and find the resolution and accuracy.	3
12	Convert analog signal to digital using suitable ADC IC and observe the output for various inputs and find the resolution and accuracy.	3
	Two CIE/IA Tests	6
	Total	**66**

Unit – 2: Student Activities [CIE- 05 Marks] 06 Hours

Sl. No.	Activity	Duration (Hr.)
1	Collect the information on the memory system of a computer used in the lab.	**3**
2	Simulate the working of any simple logic circuit using a suitable modern software tool.	**3**

Institutional Activity (No marks)

The following are suggested institutional activities, to be carried out at least one during the semester. The course teacher/coordinator is expected to maintain the relevant record (Containing, Activity name, Resource persons and their details, duration, venue, student feedback, etc) pertaining to Institutional activities

Sl. No.	Activity
1	Organize hands-on practice on design and simulation of digital circuits.
2	Motivate student to take case study on different ASICs (Application specific ICs) digital circuits to inculcate self and continuous learning.

References

1. *Digital Principles and Applications*, Donald P Leach, Albert Paul Malvino, Goutam Saha, McGraw-Hill publications.8e
2. *Digital Systems Principles and Applications*, Ronald J. Tocci, Neal S Widmer, Gregory L. Moss. Pearson Publication.

3. *Digital Electronics –principles and Integrated circuits* ,Anil K.Maini,wiley India edition.
4. https://www.circuitlogix.com
5. http://www.vlab.co.in/
6. www.electronicforu.com/
7. www.electronicprojects.org/
8. http://www.asic-world.com/
9. http://www.freebyte.com
10. http://www.electronics-tutorials
11. http://www.circuitstoday.com
12. http://www.allaboutcircuits.com

Course Delivery

The course will be delivered through two-hour tutorials and four-hour hands-on practice per week. Tutorial shall be imparted before the conduction of the experiment. Student activities are off-class and presentation/report evaluation is during assigned lab sessions.

Course Assessment and Evaluation Scheme

Master Scheme

Assessment Method	What		To Whom	Assessment mode /Frequency /timing	Max. Marks	Evidence Collected	Course Outcomes
Direct assessment	CIE	IA	Students	Two tests+	10	Blue Books	1 to 6
				Record@	10	Record Book	1 to 6
				Activity*	05	Report/Sheets	1 to 6
	SEE	End exam		End of the course	50	Answer Scripts at BTE	1 to 6
				Total	75		
Indirect assessment	Student feedback on course		Students	Middle of the Course	Nil	Feedback Forms	1 to 3 Delivery of course
	End of course survey			End of the Course	Nil	Question-naires	1 to 6 Effectiveness of delivery instructions & assessment methods

Legends: CIE-Continuous Internal Evaluation, SEE- Semester End-exam Evaluation

I.A. test shall be conducted as per SEE scheme of valuation. However obtained marks shall be reduced to 10 marks. Average marks of two tests shall be rounded off to the next higher digit.
Rubrics to be devised appropriately by the concerned faculty to assess Student activities.

***S**tudents should do activity as per the list of suggested activities/ similar activities with prior approval of the teacher. Activity process must be initiated well in advance so that it can be completed well before the end of the term.

@ Record Writing: Average of marks allotted for each experiment; fractional part of average shall be rounded off to next higher integer.

Composition of CLs

Sl. No.	Cognitive Levels (CL)	Weightage (%)
1	Remembering	25
2	Understanding	40
3	Applying	35
	Total	**100**

Continuous Internal Evaluation (CIE) pattern

(i) Student Activity (5 marks)

The student activities in Unit-2 or similar activities can be assigned

Execution Notes:

1. Activities are assigned batch-wise (maximum of 2 students per batch); any one activity/project per batch should be assigned by the teacher based on interest of the students. Student can also choose any other similar activity with a prior approval from the concerned teacher.
2. Teacher is expected to observe and record the progress of students' activities
3. Assessment is made based on quality of work as prescribed by the following **rubrics** table.

(ii) Model of rubrics for assessing student activity (for every student)

Dimension	Scale					Marks (Example)
	1 Unsatisfactory	2 Developing	3 Satisfactory	4 Good	5 Exemplary	
1. Research and gathering information	Does not collect information relate to topic	Collects very limited information, some relate to topic	Collects basic information, most refer to the topic	Collects more information, most refer to the topic	Collects a great deals of information, all refer to the topic	3
2. Full-fills team roles and duties	Does not perform any duties assigned to the team role	Performs very little duties	Performs nearly all duties	Performs almost all duties	Performs all duties of assigned team roles	2
3. Shares work equality	Always relies on others to do the work	Rarely does the assigned work, often needs reminding	Usually does the assigned work, rarely needs reminding	Always does the assigned work, rarely needs reminding.	Always does the assigned work, without needing reminding	5
4. Listen to other team mates	Is always talking, never allows anyone to else to speak	Usually does most of the talking, rarely allows others to speak	Listens, but sometimes talk too much,	Listens and talks a little more than needed.	Listens and talks a fare amount	3
					Total marks	ceil(13/4)= 4

(iii) CIE/IA Tests (10 Marks)

Two tests have to be conducted in accordance SEE pattern and the marks shall be scaled down to 10. Average of two tests, rounding-off any fractional part to next higher integer, shall be considered for CIE/IA.

(iv) Record Evaluation (10 Marks)

Every experiment shall be assigned marks for a scale of 10 after its conduction based on student's performance and quality of write-up. Average of them, by rounding-off any fractional part to next higher integer, shall be considered for CIE/IA.

Semester End-exam Evaluation (SEE) Scheme

Sl. No.	Scheme	Max. Marks
1	Writing two circuit diagrams (one from part A and one from part B) with applicable Procedure / Tabular/ Ideal graph/ formula for calculations	20
2	Construction and conduction of any one circuit	15
3	Result	05
4	Viva-voce	10
TOTAL		**50**

Note:
1. Candidate is expected to submit the Lab record for the examination
2. Student shall not be allowed to conduct directly if he/she is unable to write at least one correct circuit diagram

Laboratory Resource Requirements

Hardware Requirement: For a batch of 20 students

Sl. No.	Equipment	Quantity
1	Digital trainers	10
2	Dual trace oscilloscope.	05
3	Digital multimeters	05
4	ICS-7400,7402,7404,7408,7432,7486,7442,7445,7446,7474,7476,7427,7489,7490,7494,7495,74141,74148,74153,74157,74155,74193,74194,DAC0808,ADC-0800,741,555 timer	10 each
5	Patch cards(different lengths)	250
6	Digital IC Tester	02

Model Questions for Practice and Semester End Examination

N**ote:** The questions in the question bank are indicative but not exhaustive.

GROUP A

1. Verify the functionality of 4:1 or 2:1 multiplexer choosing suitable IC.
2. Design and verify the equation y =$\bar{A}$B+A$\bar{B}$ using suitable multiplexer IC.
3. Modify a 2:1 multiplexer IC to work as a 4:1 multiplexer and show the operation.
4. Demonstrate the operation of a decoder circuit.
5. Design a circuit to display decimal numbers on a common anode/cathode seven segment display..
6. Verify the functionality of an encoder circuit.
7. Verify the operation of a decimal to BCD encoder.
8. Verify the read and write operation on a RAM using suitable IC.

9. Construct Astable multivibrator using timer IC 555 to generate square output waveform for a frequency.
10. Construct Astable multivibrator using timer IC 555 with $R_A = R_B$=1k ohms and c= 1000 microfarads and compare the theoretical and practical frequency of oscillation.
11. Construct Monostable multivibrator using timer IC 555 to generate pulses for a given ON periods.
12. Use timer IC 555 as a one shot and show the output waveform.

GROUP B

13. Choose suitable logic gates to construct and identify the output of an S-R FF.
14. Verify the operation of a clocked S-R FF.
15. Verify the operation of a J-K FF.
16. Verify the operation of a J-K FF and show the role of preset and clear inputs.
17. Verify the operation of a D FF.
18. Verify the operation of a T FF.
19. Convert JK FF to a D FF and verify the operation.
20. Modify JK FF to a T- FF and show that it divides the clock input frequency by 2.
21. Verify the operation of SISO shift register.
22. Verify the operation of SIPO shift register.
23. Verify the operation of PISO shift register.
24. Verify the operation of PIPO shift register.
25. Verify the operation of 3-bit asynchronous Up-counter.
26. Verify the operation of 3-bit asynchronous down-counter.
27. Verify the operation of mod-10 counter with the help of IC 7490.
28. With the help of IC 7474, construct a 3-bit ring counter and verify the operation.
29. With the help of IC 7474, construct a 3-bit Johnson's counter and verify the operation.
30. Design and verify the working of mod-5 asynchronous counter using FFs.
31. Design a mod-3 synchronous counter and verify the operation.
32. Use DAC 0808 or any other similar ICs and tabulate the output for different values of inputs.
33. Use ADC 0800 or any other similar ICs and tabulate the output for different values of inputs.

End